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In re the application of Lee D. Whetsel — TI-14124D.6

Div. of Serial No. 10/649,274 — Prev. Art Unit: 2131

Filed:10/20/2003 — Prev. Examiner: Hua, L.

Title: Digital Bus Monitor Integrated Circuits

Information Disclosure Statement A

October 22, 2003

Asst. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as Express Mail airbill EV333320875US in an envelope addressed to: Assistant Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on October 22, 2003.

Lawrence J. Bassuk, Reg. No. 29,043

Applicant requests consideration of all patents, publications or other documents listed on enclosed forms PTO-1449A.

Under Rule 97(h), the filing of this information disclosure statement shall not be construed to be an admission that the information cited in this statement is, or is considered to be material to patentability as defined in Rule 56(b).

Applicant points out particular references and figure numbers and provides a brief explanation of each cited reference in Attachment A.

Please consider this statement as filed under Rule 97(b) within three months of the filing of a national application, or before the mailing date of a first Office action on the merits, which ever event occurs last. No certification or fee is due. We enclose two copies of this sheet.

Respectfully submitted,

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Attachment A

Foreign Patent Documents

EP 0,310,152 A2 (European patent application) to Wood discloses a synchronous test overlay circuit, Figure 3, interposed between blocks of logic to be tested.

JP 01-038674 A discloses eliminating the need for an additional input terminal for testing by providing a test recognition circuit 9.

JP 01-043773 (A) to Koji discloses testing a propagation delay to a flip-flop 104 by selecting the output of flip-flop 104 with a scan-address pin 112 to obtain the state of the flip-flop 104 output on scan-out pin 116.

JP 01-068167 A discloses a fault detection processor. Signal checking means 2 detects the presence and absence of an error. Fault occurrence calculation means 3 calculates a fault occurrence frequency PF. Device test start means 4 starts a devices test circuit 9 as the frequency PF is a prescribed value or more.

JP 64-079,673 to Masao discloses testing a RAM circuit.

JP 01-110,274 (A) discloses a serial scan path between terminals 91 and 95, see Figure 1. Each of registers 100 (101-108) has three inputs: one serial input, a parallel input from the output of circuit block 10X and an input from the output of circuit block 10A. Shift registers 80A and 80D also are connected in the serial scan path.

JP 57-094857 A apparently discloses a scan path 471-472 with three sets of latches 400-403, 410-413, and 430-433. Addresses are supplied to latches 400-403. The contents of the scratch pad memory is read to latches 430-433, which are then observed by shifting.

JP 57-209546 (A) discloses flip-flops 2-1 through 2-n, storage registers 3A and 3B, multiplexers 4A, 4B and 4C, a comparison condition setting flip-flop 5 and a comparison circuit 6. Storage registers 3A and 3B contain scanning addresses loaded externally. Multiplexers 4A and 4B selectively output the contents of the flip-flops 2-1 through 2-n according to the addresses stored in them. Multiplexer 4C outputs the contents of the selected flip-flop according to the addresses present on address line l.

JP 58-155599 to Wada, et al. discloses a memory testing circuit.

JP 58-191021 A discloses detecting a fault in comparator 3 by comparing the received input interface 2 with a standard input stored in memory 1.

JP 59-210382 (A) discloses testing an LSI circuit with scan-in flip-flops 23aa-23ag and scan-out flip-flops 23ba-23br. Testing device 1 provides an address decoded in decoder 25 to select one scan-in and one scan-out flip-flop. The outputs of the flip-flops are connected through an OR gate 26 to a testing device, which compares the outputs to decide whether the LSI is normal.

JP 60-140834 discloses that the comparison circuit 2 compares the outputs of the 4 bit register 1 with the expected data outputs of register 3.

JP 60-0252958 discloses scan flip-flops 35a-35c in each input/output circuit unit 31. Necessary data are transmitted in series using a small number of connecting lines distributed by a decoder 34.

JP 60-262073 discloses monitoring the operation of digital signal processor 1 by simulation processor. Input data on input signal line IL is stored in memory 6. Output from the digital signal processor 1 is stored in memory 7. Simulation processor 8 processes the data from memory 6 and the output of processor 8 is compared in comparator 3 with the data stored in memory 7. Non-coincidence causes a signal on terminal 5.

JP 62-031447 A discloses monitoring and recording data on a data bus independent of a computer to be monitored. The monitored data is compared with other data to determine stop conditions.

JP 62-228177 (A) discloses circuits 11-13 that capture the logical states on terminals 1-4. The contents of circuits 11-13 can be clocked out on terminal 23 by placing a low on terminal 4.

JP 62-280663 discloses logic circuit 110. Fault detection circuits 121-12n detect faults in logic circuit 110 at particular locations. Flip-flops 141-14n save the detected fault state through selectors 131-13n. Logic circuit 150 receives the outputs of flip-flops 141-14n and produces a fault signal at terminal C.

JP 63-073169 (A) discloses reducing by one pin the number of pins used for normal and test operation. Pin 6 is multiplexer for both data and test.

JP 63-188783 A discloses a logic analyzer. A detector 10 detects a prescribed logic relation among plural binary inputs. Time width detection part 20 determines whether the prescribed logic relation occurs for a prescribed time. Selection part 30 selects a prescribed input signal to be analyzed.

JP 63-213014 A discloses shift path control means 100 passing an instruction to clock transmission instruction means 200 that controls transmission of a clock signal to each of 1st shift

path logical units 400,410, 2nd shift path logical units 420,430,440, and 3rd shift path logical unit 450.

JP 63-310046 A discloses a test auxiliary circuit. The circuit reduces a serial shift operation to read out response data of a circuit to be tested by latching data at an input terminal to a latch circuit only when the data at a parallel input terminal differs from expected value data.

JP 64-006572 discloses in Figure 1 an Exclusive-OR gate 8 receiving the outputs of input shift registers 2 and output shift registers 5.

Other Documents

The Avra paper discloses a test and maintenance control block that receives commands serially over an ETM-BUS to control chip level test and maintenance features such as chip initialization, serial scan, debug and built-in self-test operations.

The Bhavsar, et al. paper (1981) discloses self testing by polynomial division in feed back shift registers for test vector generation and response evaluation.

The Breuer, et al. paper discloses a module test and maintenance controller (MMC) for testing chips. The controller tests every chip in a module by an ETM-BUS or a Boundary Scan bus. The MMC requires either a RISC-type processor or DMA controller.

The Dervisoglu paper discloses an architecture for implementing scan technology for test and debug in a sate-of-the-art workstation.

The El-ziq, et al. paper discloses a mixed-mode built-in self-test technique using scan path and signature analysis.

The ETM-Bus Specification paper discloses the performance requirements for a particular test bus.

The Haedtke, et al. paper discloses multilevel self-test for the factory and field. Figure 4 depicts a simplified bi-directional boundary scan I/O cell.

The Hahn, et al. paper discloses VLSI testing by on-chip error detection with scanned and expected data being latched in respective latches. The outputs of the two latches connect to an exclusive OR gate to determine any error.

The Hudson, et al. paper, September, 1987, discloses parallel self test with pseudo-random test patterns.

The Hudson paper discloses integrating BIST and boundary scan on a board.

The IBM Technical Disclosure Bulletin, June, 1985, discloses a bi-directional double latch that can be used in Level Sensitive Scan Designs.

The IBM Technical Disclosure Bulletin, December, 1988, discloses a self-contained performance monitor for a personal computer. The monitor interrogates the PC I/O for 2 programmable events and 1 external event. When an event occurs, a timer value, the PC data bus, and identification information are captured and automatically gated into a battery-back-up RAM. The RAM is read through a register 60 connected to a register bus.

The Intel 80386 Programmer's Manual discloses the debugging features of the 80386 architecture and the registers used for debugging. The principal debugging support takes the form of debug registers. The debug registers support both instruction breakpoints and data breakpoints.

A reserved debug interrupt vector permits the processor to automatically invoke a debugger task or procedure when an event occurs that is of interest to the debugger. The debug registers are accessed by variants of the MOV instruction.

The Intel386™ DX Microprocessor data sheet discloses the debugging features of the 80386 architecture and the registers used for debugging. On the page of the data sheet following the page carrying Fig. 2-13, Debug Registers, and at the paragraph bridging the left and right columns, the data sheet explains that the Debug registers can only be accessed in Real Mode. At Section 3.1, REAL MODE INTRODUCTION, Real Mode operation allows access to the 32-bit register set of the 80386.

The Intel Microprocessor and Peripheral Handbook, Section 2.11.2 TLB Testing, also discloses that there are two TLB (Translation Lookaside Buffer) testing operations. One is to write entries into the TLB. The other is to perform TLB lookups. C: is the command bit. A "0" written into this bit causes an immediate write into the TLB entry. A "1" written into this bit causes an immediate TLB lookup.

The Joint Test Action Group paper, January, 1988, discloses an early version of the standard for a boundary scan test architecture.

The Kuban paper discloses a built-in self-test of a Motorola microprocessor having a serial architecture. The self-test is based on a ROM-driven signature analysis technique. The resulting signature is output from the microprocessor for external examination of the signature.

The Laurent paper discloses implementing a boundary scan path and an internal scan path in VLSI circuits. Figures 2 and 3 depict respective input and output buffers.

The Lien paper discloses a Module test and Maintenance Controller (MMC) that can test every chip on a JTAG boundary scan bus and control more than one test bus. The MMC includes a test-channel that, once initialized by the MMC processor, controls testing across a specific test bus.

The Marlett, et al. paper discloses a RISP methodology for testing integrated circuits.

The Maunder et al. paper discloses an industry-standard boundary-scan framework for merchant and custom integrated circuits. The boundary-scan path provides for external, internal and self-testing of integrated circuits through shift register-latch scan-cells located at the bond pads of the integrated circuit. Figure 9 depicts one possible implementation of a scan-cell complying with JTAG requirements. The paper also discloses testing analog signals.

The Ohletz, et al. paper discloses investigating the overhead for different scan designs and self-testing designs.

The Ohsawa, et al. paper discloses a 4 Mbit CMOS DRAM with built-in self-test. A board carrying 64 4 Mbit x 1 DRAMs provides for simultaneous testing of all DRAMs in one row.

The Paraskeva, et al. paper discloses a new structured test register for VLSI self-test. See Figure 1.

The Pradhan et al paper discloses a circular BIST technique to perform a random test of sequential logic. Additional deterministic tests are presented to the circuit under test by configuring the circular path as a partial scan chain.

The Russell paper discloses the JTAG proposal and it impact on automatic testing. Figure 2 depicts an input pin cell and Figure 3 depicts an output pin cell.

The Sabo paper discloses the costs of not designing for test.

The Sellers, et al. book extract illustrates four ways to design an error correction circuit in Figures 12.2a-12.2d.

The van Riessen, et al. paper discloses integration of the boundary scan standard with the built-in self test approach. The built-in self test uses a macroprocessor, see Figure 7 to produce a test signature.

The Wagner paper discloses interconnect testing with boundary scan. Figure 4 depicts a boundary scan bit-slice.

The Wang, et al. 1986 paper discloses a concurrent built-in logic block observer combines the scan and BILBO techniques.

The Wang, et al. 1989 paper discloses using a JTAG boundary scan bus with pseudorandom patterns from a cellular automaton to locate defective chips and walking sequences to locate bad interconnects.

The Whetsel paper, January, 1988, discusses the details of the JTAG port and architecture. Figure 8 depicts a boundary register bit.

The Whetsel paper, July, 1988, discloses a standard test bus and boundary scan architecture used by Texas Instruments Incorporated in its implementation of the JTAG architecture. The disclosure covers the scan path, a scan cell, a test access port and instruction and data registers, and state diagrams.

The Whetsel paper, October, 1988, discloses a proposed standard test bus and boundary scan architecture from the Joint Test Action Group.

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ATTY. DOCKET NO.	SERIAL NO.
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APPLICANT: Lee D. Whetsel

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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
		EP 0,310,152	4/5/1989	Europe	G01	R31/28	X
		JP 01-038674 A	2/8/1989	Japan	G01R	31/28	X
		JP 01-043773	2/16/1989	Japan	G01	R31/28	X
		JP 01-068167 A	3/14/1989	Japan	H04M	3/22	X
		JP 01-079673(A)	3/24/1989	Japan	G01R31	28	X
		JP 01-110274	4/26/1989	Japan	G01R31	28	X
		JP 57-094857 A	6/12/1982	Japan	G06F	37582	X
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		JP 60-262073	12/25/1985	Japan	G01R	31/28	X
		JP 62-031447 A	2/10/1987	Japan	G06F	37582	X
		JP 62-228177	10/7/1987	Japan	G01R31	28	X
		JP 62-280663	12/5/1987	Japan	G01R	31/28	X
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		JP 63-310046 A	12/19/1988	Japan	G06F	37606	X
		JP 64-006572	1/13/1989	Japan	G01R	31/28	X

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		IBM Technical Disclosure Bulletin, "Bidirectional Double Latch", Vol. 28, No. 1, June, 1985	
		IBM Technical Disclosure Bulletin, "Self-Contained IBM Performance Monitor for a Personal Computer", December, 1988, Vol. 3, No. 7, pp.376-377	
		Intel, "80386 Programmer's Reference Manual 1986", Chapter 12: Debugging, pp. 12-1 - 12-9, 1/18/1988	
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		Joint Test Action Group, Technical Sub-Committee, "A Standard Boundary Scan Architecture", January 1988	

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